



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,250	12/12/2003	Rino Micheloni	2110-92-3	9815
7590 03/08/2006			EXAMINER	
GRAYBEAL JACKSON HALEY LLP			LAM, DAVID	
Suite 350			ART UNIT	
155-108th Avenue N.E.			PAPER NUMBER	
Bellevue, WA 98004-5973			2827	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

HA

<b>Office Action Summary</b>	<b>Application No.</b> 10/735,250	<b>Applicant(s)</b> MICHELONI ET AL.	
	<b>Examiner</b> David Lam	<b>Art Unit</b> 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 26 May 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-18 and 21-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 4, 10, 11, 14-16, 18 and 23-25 is/are rejected.
- 7) ☒ Claim(s) 2-3, 5-9, 12-13, 17, 21-22, 26-30 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 December 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/12/03</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Pre-Amendment*

1. This office action is in response to pre-amendment file on 5/26/04
  - Claims 19-20 have been cancelled.
  - Claims 21-30 are newly added.
  - Claims 1-18, 21-30 are pending in the application.

### *Priority*

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Italy on 12/12/2002. It is noted, however, that applicant has not filed a certified copy of the MI2002A002629 application as required by 35 U.S.C. 119(b).

### *Drawings*

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: **P<sub>0</sub>- P<sub>N</sub> on page 3, line 23**. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

Art Unit: 2827

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

4. Claims 2, 11, 29-30 are objected to because of the following informalities:
- In claim 2, line 2, “detection means of address transitions such as to receive” should be change to -- address transition detection means that receiving --;
  - In claim 11, line 2, “the temperature” should be change to – a temperature --;
  - In claims 21, 27, 29, 30 lines 7-10, 7-11, 13-17, 16-19, respectively, “a detected signal transition” should change to -- a transition detection signal --, “the detected transition” should be change to – the transition detection signal --;
  - In claim 29, lines 3, 7, respectively, “raw” should be change to – row --;
  - In claim 30, pages 8-9, lines 4, 1, respectively, “raw” should be change to – row --
- Appropriate correction is required.

With regard to claims 1-18, 23-22, the claims contain numerous unclear statements.

Applicant’s attention is required to further review the claims and correct necessary correction of punctuation in order to provide a more clearly understanding of the intended claimed invention. For example: in claim 1, lines, 3-4, 6-7, respectively, “making available on a output a data ..... address signal”, “ in such a way as to ..... data to be read”; in claim 2, line 2, “detection means of address transition such as to receive ..... as input”; in claim 14, lines 1-4, “ comprising a device ..... the timing signal; in claim 18, lines 13-17, “to proceed values the respective delay times or

Art Unit: 2827

..... when all delay signals have proceed value”; in claim 23, lines 5-6, the phrase “for or approximately for”.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 4, 10, 14, 16, 23-24 as understood by Examiner are rejected under 35 U.S.C. 102(b) as being anticipated by Takeda (5,978,891).

Regarding to claims 1, 4, Takeda discloses a memory system comprising a semiconductor memory (401) for storing digital data, the memory connected to a control device (400) for receiving an address signal; a generating circuit (402) for activating a wait signal to be send to the control device during reading operations to indicate non availability of the data to be read, and for deactivating the wait signal to indicate the availability of the data to be read, after a waiting time interval correlated with the actual access time of the memory, wherein the waiting time interval having a duration that is variable as a function of the address signal and of at least one operative parameter of the memory system; wherein the generating circuit comprising end-wait signaling (wait counter/count setting) means for generating an end-wait signal (set to false), following the wait interval, which control the deactivation of the wait signal. *See at least Figs. 3-4; for example Cols. 7-9, lines 42-67, 1-67, 1-12, respectively, and the related disclosure.*

Regarding to claims 10, 14, 16, Takeda discloses the memory system further comprising at least one operative parameter comprises a memory supply voltage (for example of Cols. 14, lines 26-55); a control timing signal device for generating control timing signal, wherein the generating circuit to activate and deactivate the wait signal in an asynchronous manner with respect to the timing signal (for example of Cols. 7-8, lines 39-67, 1-6, 39-63); wherein the memory is arranged according to a plurality of the rows, columns and words (cell array 100).

Regarding to method claims 23-24, Takeda discloses a memory system capable of accessing a memory by transitioning bit in multiple section of an address signal the sections respectively correspond to domains (rows, columns) of the memory; the domains having

Art Unit: 2827

respective delays; preventing subsequent access to the memory (stop read or write) on the longest of the access delay timing ( $t_2$ ); wherein the access delays are dependent on supply voltage (for example of Cols. 14, lines 26-55). *See at least Figs. 3-4; for example Cols. 7-9, lines 42-67, 1-67, 1-12, respectively, and the related disclosure.*

6. Claims 18, as understood by Examiner rejected under 35 U.S.C. 102(e) as being anticipated by Jeon (6,385,078).

Regarding to claim 18, Jeon discloses a wait circuit (320, 330) for a memory having multiple domains sections (RAi/RaiB, CAi/CAiB) that respectively delay times; the wait circuit comprising an address transition detection circuit (ATD) operable to receive an address signal having multiple sections that respectively correspond to the domains, to detect respective signal transitions in the sections, and to generate a respective transitions detect signal (ATD\_SIG') in respond to the signal transitions; a delay circuit (330) coupled to the address transition detection circuit and operable to transition a wait signal (delay signal) to a wait value in respond to the generation of a transition detection signal (ATD\_SIG); wherein the respective delay signal is delayed for a predetermined delay time by the delay circuit. *See at leas Figs. 4-6; for example Cols. 5-6, lines 5-67, 1-65, respectively, and the related disclosure.*

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Art Unit: 2827

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 11, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda (5,978,891) in view of Mori et al. (6,748,464).

Takeda disclose all the elements of the memory system as applied in claim 1, 23 above.

Takeda lack an inclusion of wherein at least one operative parameter comprises the temperature at which the memory system operates.

Mori et al. disclose a memory system comprising semiconductor memory (9) coupled to a control device (2); wherein at least one operative parameter comprises a temperature at which the memory system operates. *See Fig. 1, for example Cols. 4-5, lines 7-17, 12-27, respectively, and the related disclosure.*

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Takeda's memory system to include at least on parameter comprises the temperature at which the memory system operates as taught by Mori et al. in order to provide high-speed processing capability in a memory system.

8. Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda (5,978,891) in view of Hansen et al. (5,822,244).

Takeda disclose all the elements of the memory system as applied in claim 1 above.

Takeda lack an inclusion of wherein the memory comprises a flash memory.

Hansen et al. disclose a flash memory (12) coupled to a control device (10) for receiving address signals. *See at least Fig. 1.*



It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Takeda's memory system by provide a flash memory as taught by Hansen in order to provide a high-speed, less power consumption and low cost semiconductor memory system.

***Allowable Subject Matter***

9. Claims 2-3, 5-9, 12-13, 17, 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the generating circuit as noted in claim 1 above, and wherein the generating circuit further comprises address transition detection means that receive the address signal as input and generating an address transition detection signal representing a modification thereof, wherein the generating circuit activate the wait signal in response to the address transition detection signal; the method as noted in claim 23 above, and further comprising step of allowing subsequent access to the memory when all the delay signals have proceeded value, and among others as claimed in claim 26.

Claims 21-22, 27-30 would be allowable if rewritten or amended to overcome the objection, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach a wait circuit, among others as claimed in independent claims 21, 27, 29, 30, operate to transition a wait signal to a wait value in response to a transition

Art Unit: 2827

detection signal and to transition the wait signal to a the proceed value after or approximately after the longest one of the delay times that correspond to the transition detection signal.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00 – 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852852. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**D. Lam**

March 4, 2006



**DAVID LAM**  
**PRIMARY EXAMINER**